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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,812	11/09/2001	Dan Nobbe	CS11202	9495

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EXAMINER	
JAMAL, ALEXANDER	
ART UNIT	**PAPER NUMBER**
2643	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,812	NOBBE ET AL.	
	Examiner	Art Unit	
	Alexander Jamal	2643	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Based upon the submitted amendment (12-28-2005), the examiner notes that no claims have been amended, only arguments presented.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 12,8,13,14,19,3-5,7,9,10,12,15-17,20** rejected under 35 U.S.C. 103(a) as being unpatentable over Wagemans et al. (6697606), and further in view Donig et al (5524037).

As per **claim 1,** Wagemans discloses a transceiver that may be used in a direct communications system (Col 1 lines 10-60). The transceiver comprises a reference oscillator signal (means 6 in Fig. 1) coupled to divider means 7. The divider means can be any set of 2 dividers, or 3 dividers in series (Col 2 lines 2-18). Furthermore, the reference signal may be applied to frequency multipliers (along with the dividers) to produce the required frequency (Col 2 lines 60-67). However, Wagemans does not disclose the specific arrangement of a frequency doubler coupled to a divide by 3 circuit,

with the output and a delayed version of the output coupled to an AND gate in order to adjust the duty cycle of the output waveform.

In Wagemans system, the divider means can be any set of 2 dividers, or 3 dividers in series (Col 2 lines 2-18). Furthermore, the reference signal may be applied to frequency multipliers (along with the dividers) to produce the required frequency (Col 2 lines 60-67). It would have been obvious to one of ordinary skill in the art at the time of this application that an combination of frequency multipliers and dividers could be implemented in series for the purpose of producing the correct operating frequency from a given reference oscillator in order to implement a predetermined communications standard.

Donig discloses that frequency dividers will often leave the output signal with a non-harmonically-optimum duty cycle (ie. not 50%). Donig discloses that a delayed version of an output signal can be delayed and the original and delayed output signals can be fed into a logic gate in order to adjust the duty cycle (Col 1 line 40 to Col 2 line 31). It would have been obvious to one of ordinary skill in the art at the time of this application that a logic gate (AND or OR) could be used with the output signal and delayed output signal in order to recover the duty cycle from any frequency division operations.

As per **claim 8,** claim rejected for same reasons as claim 1 rejection.

As per **claim 13,** claim rejected as a method performed by the device of claim 1 rejection.

As per **claims 2,14,19,** Wagemans's system in view of Donig's teachings comprises a divide by three circuit (Donig: Fig. 1). In the circuit, the delay device (6) is clocked by the same signal (1) input into the frequency divider. If Wageman's system were to implement a fractional dividing circuit (such as 2/3) then the delay generating means would be clocked by the input to the divide by 3 circuit.

As per **claims 3,9,20,** claim rejected for same reasons as claim 2 rejection. The delay period is ½ clock cycle in order to return the duty cycle to 50% (Donig: Col 2 lines 1-12).

As per **claims 4,5,10,16,17,** the gate is an AND gate and the delay circuit is a D flip flop (Donig).

As per **claims 7,12,15,** Donig discloses that the divide by three circuit has a 2/3 duty cycle (Col 1 lines 10-30).

4. Claims 6,11,18, rejected under 35 U.S.C. 103(a) as being unpatentable over Wagemans et al. (6697606) and Donig et al (5524037) as applied to claims 1,8,13, and further in view of Lehtinen (5983081).

As per **claims 6,11,18,** Wageman's and Donig disclose applicant's claims1,8,13, but they do not specify an additional switchable frequency doubler coupled to the frequency division circuitry. Lehtinen discloses a direct conversion receiver with a selectable frequency multiplier (28,31 in Fig. 2) used to produce a reference signal used in the system. Lehtinen teaches that implementing a frequency multiplier (such as a doubler) would allow for a reduction in frequency synthesizer in the case where the

transceiver is used for multiple protocols (such as PCN and GSM) (Col 1 line 40 to Col 2 line 29). It would have been obvious to one of ordinary skill in the art at the time of this application that the reference frequency could be switchably doubled for the purpose of allowing the system to more efficiently handle multiple signaling protocols.

Response to Arguments

5. Applicant's arguments with respect to **claims 1,8,13** have been considered but are not persuasive.

As per applicant's arguments that Wageman does not disclose frequency multipliers and frequency dividers (remarks page 6), examiner disagrees. Wageman discloses a direct conversion telecommunications device that comprises clock generating circuitry. Wageman specifically notes that any number of well known logic circuits (including multipliers and dividers) may be combined in series to produce a desired frequency. Wageman (Col 2) specifically teaches that various combinations of dividers/multipliers may be used to produce a desired clock frequency. Examiner contends that one skilled in the art, based upon Wageman's disclosure would make the obvious choice of providing the appropriate multiplier/divider circuits in order to produce a desired clock frequency.

As per applicant's argument (remarks page 6) that that the Donig reference is not properly combined with the Wageman reference, examiner disagrees. The prior office action cited specific motivation to implement the duty-cycle controlling circuitry taught by Donig with the divider circuits disclosed by Wageman. There is clear motivation (as noted in the claim 1 rejection above) to restore the signal duty cycle in situations where

frequency divider circuits are used. The duty cycle restoring circuitry would obviously have been implemented after any dividing circuits implemented in Wageman's system.

As per applicant's argument that it is not clear how the Lehtinen reference would be combined with Wageman and Doing (remarks page 6), examiner disagrees. Lehtinen teaches the use of a switchable frequency multiplier that may be implemented in a telecommunications device in order to allow the device to handle a greater set of protocols (each protocol requiring different clocking frequencies). The switchable multipliers taught by Lehtinen would obviously be implemented as part of (in series with) the frequency generating circuitry disclosed by Wageman in order to allow for a greater range of frequencies to be generated by the circuitry (which would allow for a greater number of protocols to be used).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Jamal whose telephone number is 571-272-7498. The examiner can normally be reached on M-F 9AM-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curtis A Kuntz can be reached on 571-272-7499. The fax phone numbers for the organization where this application or proceeding is assigned are **571-273-8300** for regular communications and **571-273-8300** for After Final communications.

AJ
January 18, 2006